Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. An electro-static discharge (ESD) protection circuit for a dual polarity input/output(I/O) pad, comprising:
a substrate of first type;
a deep well region of second type, disposed in the substrate of first type;
a well region of first type, disposed in the deep well region of second type;
a first transistor, disposed over the well region of first type, wherein the first transistor comprises a first gate, a first source and a first drain;
a second transistor, disposed over the substrate of first type, wherein the second transistor comprises a second gate, a second source and a second drain, wherein the second source is connected withthe first drain, and wherein the second source and the first drain is disposed in a portion of the first type well region, a portion of the second type deep well region and a portion of the first type substrate;
a first doped region, disposed in the well region of first type and laterally adjacent to the first source, wherein the first doped region, the first source and the first gate are electrically connected to an input pad; and

a second doped region, disposed in the substrate of first type and laterally adjacent to the second drain, wherein the second doped region, the second drain and the second gate are electrically connected to an output pad.

[c2] 2. The electro-static discharge (ESD) protection circuit of claim 1, wherein the substrate of first type comprises a p-type substrate.

[c3] 3. The electro-static discharge (ESD) protection circuit of claim 1, wherein the deep well region of second type comprises a n-type deep well region.

[c4] 4. The electro-static discharge (ESD) protection circuit of claim 1, wherein the well region of first type comprises a p-type well region.

[c5] 5. The electro-static discharge (ESD) protection circuit of claim 1, wherein the first transistor and the second transistor comprise a NMOS transistor.

[c6] 6. The electro-static discharge (ESD) protection circuit of claim 1, wherein the first doped region and the second doped region comprise a p-type doped region.

[c7] 7. The electro-static discharge (ESD) protection circuit of claim 1, wherein when the input pad receives a positive electro-static current, a first parasitic bipolar junction

transistor is formed by the first type well region, the second type deep well region and the first type substrate, and a second parasitic bipolar junction transistor is formed by the second type deep well region, the first type substrate and the second drain, and a positive feedback loop is formed by the first parasitic bipolar junction transistor and the second parasitic bipolar junction transistor.

[c8] 8. The electro-static discharge (ESD) protection circuit of claim 1, wherein when the input pad receives a negative electro-static current, a first parasitic bipolar junction transistor is formed by the first type substrate, the second type deep well region and the first type well region, and a second parasitic bipolar junction transistor is formed by the second type deep well region, the first type well region and the first source, and a positive feedback loop is formed by the first parasitic bipolar junction transistor and the second parasitic bipolar junction transistor.